SLX FPGA Release Notes 2020.2

SILEXICA

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SLX contains third-party open-source software components. The full list of third-party software components and their licenes can be found in the `data/third-party-licenses` sub-directory of the **SLX** installation and online at https://www.silexica.com/tps/.

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Revision History

Date	Version	Revision
12/03/2019	2019.1	Official Release
18/07/2019	2019.2	Official Release
08/08/2019	2019.2-sp1	Service Pack
27/09/2019	2019.2-sp2	Service Pack
10/12/2019	2019.4	Official Release
31/01/2020	2019.4-sp1	Service Pack
31/03/2020	2020.1	Official Release
06/05/2020	2020.1-sp1	Service Pack
25/06/2020	2020.2	Official Release

Typographic Conventions

This manual uses specific typographic conventions. The following table summarizes how font styles are used to emphasize important elements throughout the text.

Style	Usage
Bold	Names of Silexica products, such as **SLX for FPGA**
`Typewriter`	Literal input, e.g., user input from the command line and actual code listings
Slanted	To introduce terminology used in the Silexica (SLX) series of products

Special symbols are used to denote useful information, a remark, a warning, an expected failure or a requirement for user interaction. They are used within a shaded box with rounded corners.

Symbol	Meaning
	Useful tip
☞	A noteworthy point or remark

	A warning on tool-specific behavior
	An expected error or failure
	Required input
	Required selection of choices

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2020.2 Release

1.1 Introduction

This document gives an overview of the new and exciting features of **SLX FPGA** 2020.2, as well as information on migrating from previous releases.

For information on the previous release of **SLX FPGA**, click here for the release notes for the **Previous Release of SLX**.

1.2 New Features

For in-depth details on the new features mentioned below, please refer to the **SLX FPGA User Guide**.

- Vivado HLS projects can now be imported automatically to **SLX FPGA**. The design and testbench, as well as settings including the compiler invocation, platform/FPGA Part, clock frequency and top-level hardware function will be carried over to the created **SLX FPGA** project.

- The time that is required to analyze and extract the existing parallelism in an input design has been significantly improved. This improves turnaround times, especially when performing several design iterations.

- The default C/C++ language standard (C++98) of the **SLX** compiler now matches the one used in Xilinx Vivado HLS; the user no longer need to use custom compilation options for code that works on Vivado HLS.

- The *Interface* configuration in the *Function Mapping Editor* has been extended for additional interface types, including `BRAM`, `ap_memory` and `ap_bus`.

1.3 Resolved Issues

- **SLX FPGA** pragmas were not being generated for designs containing templated functions in the design code. This has been fixed for single instantiations of templated functions.
- Issues with array partitioning and reshaping, when targeting variables with `ap_int` and `ap_fixed` types has been resolved.
- **SLX FPGA** now analyzes parallelism in functions mapped to the FPGA even when their execution time is below filtering thresholds.

1.4 Compatibility Information

- When migrating a project from **SLX 2020.1** or older, it is required to reset the path to Xilinx tools (remove the path and re-select it) to fix errors in the code editor window. In addition, if a **SLX FPGA** project fails to compile after upgrading, please consider adding the `-std=<LangStandard>` flag to the build commands listed in `USER_BUILD`.
- Projects created with versions of **SLX FPGA** prior to 2020.2 may fail to be imported to the newest version of **SLX FPGA**. If the following error is encountered, please delete the *FPGA Part* in the *Configuration Editor* and re-select it.
  `[XSD::Exception] /.../.sdx/.sdxplatform: 39:10 error: element 'UserSetArea' is not allowed for content model..`
- This release of **SLX FPGA** has file formats containing profiling and analysis results that are incompatible with previous releases of **SLX FPGA**. If you are experiencing difficulties migrating an existing project that was created with an earlier version of **SLX FPGA**, perform a *Clean* of the project and try again. Please see the Known Issues and Limitations chapter of **SLX FPGA User Guide** for more details.

> Please note that the **SLX FPGA SDSoC** user flow is deprecated and will no longer be available with the next release of **SLX FPGA**.
>
> Please note that Windows 8 and lower are no longer supported.