

SLX Release Notes 2020.4

SILEXICA 

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Third-Party Open-source Software

SLX contains third-party open-source software components. The full list of third-party software components and their licenses can be found in the `data/third-party-licenses` sub-directory of the **SLX** installation and online at <https://www.silexica.com/tps/>.

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Preface

Typographic Conventions

This manual uses specific typographic conventions. The following table summarizes how font styles are used to emphasize important elements throughout the text.

| Style | Usage |
|----------------|--|
| Bold | Names of Silexica products, such as SLX for FPGA |
| Typewriter | Literal input, e.g., user input from the command line and actual code listings |
| <i>Slanted</i> | To introduce terminology used in the Silexica (SLX) series of products |

Special symbols are used to denote useful information, a remark, a warning, an expected failure or a requirement for user interaction. They are used within a shaded box with rounded corners.

| Symbol | Meaning |
|---|-------------------------------------|
|  | Useful tip |
|  | A noteworthy point or remark |
|  | A warning on tool-specific behavior |
|  | An expected error or failure |
|  | Required input |
|  | Required selection of choices |

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New Features

This document gives an overview of the new and exciting features of **SLX 2020.4**, as well as information on migrating from previous releases. For in-depth details on the new features mentioned below, please refer to our User Guides ([SLX FPGA User Guide](#) and [SLX C/C++ User Guide](#)). For information on the previous release of **SLX**, click here for the release notes for the [Previous Release of SLX](#).

- Support has been added for the Vivado flow of **Vitis HLS**. The new Vitis HLS compiler becomes the new HLS compiler in **SLX**, replacing Vivado HLS when Vitis HLS 2020.2 is selected in **SLX** Xilinx Tools configuration.
- **SLX 2020.4** introduces the first commercially available plugin to support Xilinx's **Vitis Unified Software Platform**. Designed to expand the capabilities of the Vitis HLS tool, the **SLX Plugin** enables the addition of new pragmas and compiler optimizations when designing for FPGAs using high-level synthesis. Key features of the plugin include:
 - Loop Interchange pragmas, which enables reordering of nested loops to remove dependencies that prevent improved parallelism, pipelining, and memory access regularity.
 - IR Design Optimizations that improve an HLS design's internal program representation before the RTL code is generated, helping to boost Vitis HLS' capabilities for automatic relocation of loop invariant memory accesses.
 - Transformation checks that are enabled for new pragmas and IR design optimizations preventing compiler transformation from being applied when not safe or legal.

The plugin can be enabled or disabled via the *Configuration Editor*. **SLX** will perform loop interchanges only when the transformation is legal and expected to accelerate the FPGA design. The Loop Interchange capability is only available when Vitis HLS 2020.2 has been installed alongside **SLX 2020.4** on Ubuntu 18.04.

- The profiling capability has been significantly enhanced. Prior to **SLX 2020.4**, **SLX** would report total and self cost of functions using a sequential CPU execution model. **SLX 2020.4** introduces the ability to understand the execution costs from an FPGA implementation point of view. **SLX** uses its fast estimation models to reveal how each function and loop contributes to overall latency of the design. This feature helps designers quickly determine where to focus their efforts. The cost in terms of relative latency contributions can be found in the following views:
 - The **Call Graph (formerly SW Call Graph)** now display the total cost for each function for the FPGA implementation. The display can be toggled between the FPGA and the CPU values.
 - The SLX Hints View reveals total costs down to the loop level.
- A new interactive **SLX FPGA** flow guidance walkthrough is provided in the *Welcome Page*. The walkthrough can be used for any imported or newly created **SLX FPGA** project and guides the user through the different steps of a typical **SLX FPGA** design flow. The walkthrough provides clarification for the action steps in **SLX FPGA** and the suggested next steps to follow. The walkthrough also highlights the analysis results relevant to the user at any point in the flow.
- Support has been incorporated for multidimensional array partitioning; **SLX** can now identify which array dimension would lead to the best performance when partitioned.

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Compatibility Information

This release of **SLX** has file formats containing profiling and analysis results that may be incompatible with previous releases of **SLX**. If you are experiencing difficulties migrating an existing project that was created with an earlier version of **SLX**, perform a *Clean* of the project and try again.

 To view a full list of limitations of **SLX**, please visit the *Known Issues and Limitations* chapter of the [SLX FPGA User Guide](#).

