SLX Release Notes 2020.3

SILEXICA

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Third-Party Open-source Software
SLX contains third-party open-source software components. The full list of third-party software components and their licenes can be found in the `data/third-party-licenses` sub-directory of the **SLX** installation and online at https://www.silexica.com/tps/.

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Preface

Typographic Conventions

This manual uses specific typographic conventions. The following table summarizes how font styles are used to emphasize important elements throughout the text.

Style	Usage
Bold	Names of Silexica products, such as **SLX for FPGA**
`Typewriter`	Literal input, e.g., user input from the command line and actual code listings
Slanted	To introduce terminology used in the Silexica (SLX) series of products

Special symbols are used to denote useful information, a remark, a warning, an expected failure or a requirement for user interaction. They are used within a shaded box with rounded corners.

Symbol	Meaning
	Useful tip
	A noteworthy point or remark
	A warning on tool-specific behavior
	An expected error or failure
	Required input
	Required selection of choices

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New Features

This document gives an overview of the new and exciting features of **SLX** 2020.3, as well as information on migrating from previous releases. For in-depth details on the new features mentioned below, please refer to our User Guides (**SLX FPGA User Guide** and **SLX C/C++ User Guide**). For information on the previous release of **SLX**, click here for the release notes for the **Previous Release of SLX**.

- Significant improvements to the area/performance models and optimization engine have been implemented in this release. These improvements lead to greater quality of results and increased performance across a broader set of designs.
- Port bitwidth support for the `ap_stable` interface has been added.
- The automatic synthesizability refactoring for C++ `rand` and `srand` functions have been added.
- A number of GUI enhancements have been introduced to make visualizations more clear and consistent.
- **SLX** now disables the generation of inline pragmas in dataflow regions and tasks.
- The Xilinx® Support Archive (.xsa) file format supported by Xilinx® Vivado HLS 2019.2 can now be imported to **SLX**. This is a slight variant of the Device Support Archive (.dsa) format also supported by Xilinx.
- Support has been added for Xilinx® Vivado HLS 2020.1.
- Support for Xilinx® Vivado HLS 2019.1 has been removed.
- The **SLX** Scheduling Design (also known as the **SLX** Automotive) workflow has been removed.

☞ The Xilinx® SDSoC flow was deprecated after Xilinx® Vivado HLS 2019.1. Since this version is no longer supported in **SLX**, the Xilinx® SDSoC flow has been removed in **SLX** 2020.3.

With the removal of the Xilinx® SDSoC flow, the Synthesis Mode called ‘‘`Place and Route`’’ has also been removed. In its place, the mode called ‘‘`Synthesis`’’ is now supported. See *Section 2.6.3.3 - Synthesis Strategy* of the **SLX FPGA User Guide** for more details.

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Compatibility Information

This release of **SLX** has file formats containing profiling and analysis results that may be incompatible with previous releases of **SLX**. If you are experiencing difficulties migrating an existing project that was created with an earlier version of **SLX**, perform a *Clean* of the project and try again.

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Limitations of SLX

3.1 Linking with Xilinx and External Libraries

When an application is compiled and executed in the **SLX** workspace, **SLX** links the following Xilinx libraries with the application:

- `Ip_dds_compiler_v6_0_bitacc_cmodel`
- `Ip_fir_compiler_v7_2_bitacc_cmodel`
- `Ip_xfft_v9_1_bitacc_cmodel`
- `Ip_floating_point_v7_0_bitacc_cmodel`
- `hls_math`

Note that these libraries are only automatically linked in Linux. On Windows, the libraries are currently not supported and cannot be used with **SLX**.

To link any other required libraries, the following must be explicitly added to the compiler invocation:

- `-lname` (name of the library)
- `-L/path/to/library` (local path of the library)
- `-Wl,-rpath,/path/to/library`

☞ To view the full list of limitations of **SLX**, please visit the *Known Issues and Limitations* chapter of the SLX FPGA User Guide.