

SLX - DATAFLOW PRODUCT

■ SLX - Optimized Dataflow Application Mapping and Automated Code Generation

SLX, Silexica's programming technology, analyzes, optimizes and integrates the computation and communication patterns on ANSI/ISO C (C89, C99) dataflow applications (with deterministic execution). It automatically selects the optimal mapping to heterogeneous cores and accelerators and plans logical channels to platform interconnects and memories. SLX gives the most effective memory allocation for the buffers used for inter-process communication and creates a complete spatial (where) and temporal (when) application map. SLX's unique source-to-source compiler technology generates parallel C code for individual processors on a multicore platform. Further benefits come as it automatically selects the best APIs for task management, synchronization, and communication from the run-time environments and Operating Systems of the target cores.

ANALYZE

Analyze your dataflow application and gain detailed application and target platform performance insights.

✓ Absolute code understanding

OPTIMIZE

Optimize the distribution of your application on your target platform, driven by performance, power and memory constraints.

✓ Meet challenging requirements

INTEGRATE

Integrate easy-to-use recipes and automatically generate code, instantly improving your software.

✓ Faster time to market

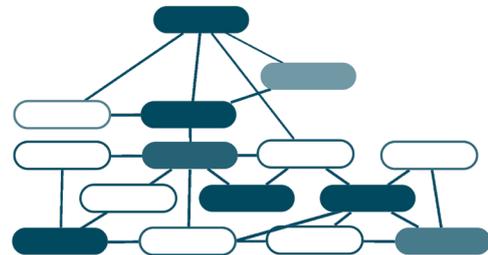
■ FEATURES AND CAPABILITIES

ANALYZE

ANALYZE CODE

Improving application distribution and communication patterns requires in-depth application knowledge. Based on unique software profiling, tracing, and microarchitecture-aware performance estimation technologies, SLX automatically extracts precise information about the behavior of applications on different target platforms, including:

- Detailed performance estimation for each process on each processing element in the target platform
- Communication patterns and memory usage
- Complete schedule for each process and processor
- Power/energy profiles for each processor
- Processor/interconnect utilization
- Intuitive dataflow visualization



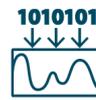
Based on interchangeable platform models and advanced performance profiling, SLX provides a rapid mapping and scheduling simulator. Unique compiler techniques statically and dynamically analyze the source code and determine platform-dependent execution costs. Using abstract processor models, the target compiler is emulated by proper instruction lowering, selection and scheduling with precision.



Static and Dynamic Source Code Analysis



Memory- and Communication Analysis



Cross-Target Performance Estimation

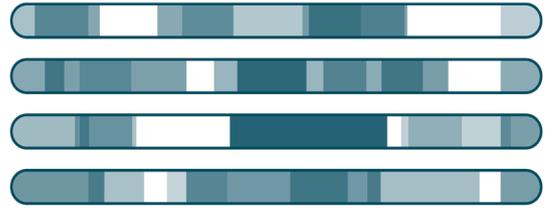


Data-flow, task-graphs

OPTIMIZE

TARGET SPECIFIC OPTIMIZATION

SLX quickly finds optimal task and communication mappings for complex applications and target platforms. It works in different optimization scenarios (Performance, Memory, Power) and fully exploits complex on-chip interconnect fabric and memory subsystems while eliminating performance bottlenecks.



Throughout the process the user can interact with the mapping flow and bring in expert knowledge like predefined task-to-accelerator or buffer-to-memory bindings and performance/power annotations.

SLX solves a range of problems that typically arise when dealing with dataflow applications such as optimal communication channel sizing, scheduling priorities and constraints. SLX enables early performance prediction and power estimation with the software without the need to purchase, install, and evaluate different available (or envisioned) multicore target platforms.



Power, performance, and memory-driven SW distribution



Optimized task schedules under tight timing constraints



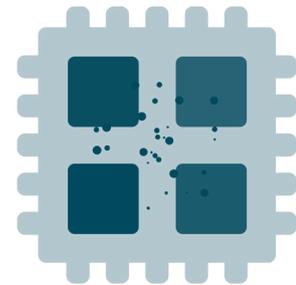
Selection of DVFS power states to decrease peak and average power

INTEGRATE

AUTOMATIC CODE GENERATION

Using SLX, source code (including instantiation, process synchronization, API calls) can be generated automatically for different target platforms.

Dataflow application can be precisely mapped to explore the capabilities of different target platforms without additional implementation overheads. The process is cost-effective, repeatable, and portable.



THE SILEXICA SOLUTION

SLX gives you absolute code understanding to meet the most challenging multicore system requirement.



Faster time to market



Mapping dependent code generation for multicores



Guaranteed quality